REMARKS/ARGUMENTS

1. In the above referenced Office Action, the Examiner rejected claims 1-4 under 35 USC § 103 (a) as being unpatentable over Appeltans (U.S. Patent No. 5,552,694) in view of Poon (U.S. Patent No. 6,188,209); claims 5, 6, 17, and 18 under 35 USC § 103 (a) as being unpatentable over Appeltans (U.S. Patent No. 5,552,694) in view of Bittner (U.S. Reissue Patent No. 37,609); claims 7 and 9 under 35 USC § 103 (a) as being unpatentable over Appeltans (U.S. Patent No. 5,552,694) and Bittner (U.S. Reissue Patent No. 37,609) in view of Poon (U.S. Patent No. 6,188,209); claims 11 and 12 under 35 USC § 103 (a) as being unpatentable over Appeltans (U.S. Patent No. 5,552,694) in view of Malcolm (U.S. Patent No. 6,373,954) and Bittner (U.S. Reissue Patent No. 37,609); and claims 19 and 20 under 35 USC § 103 (a) as being unpatentable over Appeltans (U.S. Patent No. 5,552,694) and Bittner (U.S. Reissue Patent No. 37,609) in view of Poon (U.S. Patent No. 6,188,209). The Examiner has objected to claims 8, 10, 13-16 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The rejections and objections have been traversed and, as such, the applicant respectfully requests reconsideration of the allowability of claims 1-20.

2. The applicant thanks the Examiner for considering the applicant's arguments with respect to election/restriction and for withdrawing the election/restriction requirement.

3. Claims 1-4 have been rejected under 35 USC § 103 (a) as being unpatentable over Appeltans (U.S. Patent No. 5,552,694) in view of Poon (U.S. Patent No. 6,188,209). The applicant respectfully disagrees with the Examiner's arguments supporting this rejection.

Appeltans teaches a power supply a multiple state regulation scheme. As disclosed, the regulation scheme includes five states (column 5, line 64, through column 6, line17). Appeltans teaches that the first three states correspond to a discontinuous mode of operation of the power supply and the last two states correspond to a continuous mode of operation (column 5, lines 56 – 59). Figure 5 of Appeltans illustrates the discontinuous mode of operation (i.e., the inductor current returns to zero before the next

charge cycle – e.g., switch 2 of Figure 4 being activated) and Figure 6 of Appeltans illustrates the continuous mode of operation (i.e., the inductor current does not return to zero before the next charge cycle).

Appeltans further teaches that the duration of the charge phase Φ_{i1} (i.e., switch 2 of figure 4 being active), the discharge phase Φ_{i2} (i.e., switch 11 of figure 4 being active), diode phase Φ_{i3} (i.e., switches 2 and 11 of figure 4 are open, but the diode is conducting inductor current to the load), and wait phase Φ_{i4} (i.e., switches 2 and 11 of figure 4 are open and the diode is not conducting current such that the inductor current is zero) are programmable. (column 6, line 60, through column 7, line 42) The phases are programmable via the numbers stored the storage means 7. In state 1, the charge and discharge phase are the smallest, which is intended for light loading of the power supply. As the load increases, the state changes from 1 to 2 and then to state 3. In state 2, the duration of the charge and discharge phases are increased with respect to state 1 and are further increased in state 2.

The determination as to whether to switch between states 1, 2, and 3 is made by comparing the output voltage (V_{OUT}) with a first reference voltage (V_1). The comparison is made at the beginning of the wait phase Φ_{i4} where, if V_{OUT} is less than V_1, the state is incremented by 1 (if in state 3, it is incremented to state 4) for the next charge phase. (column 7, lines 10 – 17) If V_{OUT} is greater that V_1, a wait time is observed until the output voltage as decreased below V_1, after which the discharge phase Φ_{i2} begins and the switching cycle is repeated. If, in states 1, 2, or 3, the output voltage has not decreased below V1 before the zero count is reached, the control means 10 decrements the state by 1. (column 7, lines 17 – 27)

In states 4 and 5, only the charge Φ_{i1} and discharge Φ_{i2} phases are used. At the end of the discharge phase and in state 4, the control means 10 determines whether the output voltage is in range 1 as shown in Figure 7. In this range, the output voltage is greater than the first threshold voltage and, as such, the control means decrements the state to state 3. If the output voltage is in the second range of Figure 7, the control means

maintains the state at state 4. If the output voltage is in the third range (i.e., the output voltage is below the second threshold voltage), the control means changes the state to state 5, which has a longer charge phase that state 4. (column 7, line 43, through column 8, line 50).

In state 5, the control means keeps maintains state 5 if V_{OUT} is less than V_2 and changes to state 4 if V_{OUT} is greater than V_2. In this regard, Appeltans teaches a current mode scheme of regulating a power supply by varying between continuous mode of operation and discontinuous mode of operation. In the discontinuous mode of operation, the charge, discharge, diode, and wait phases are adjusted based on the load requirements (i.e., the greater the load, the longer the charge and discharge phases, with less wait time, which is achieved by increasing the state count). In the continuous mode, the charge and discharge phases are adjusted based on the load requirements. The load requirement is determined by comparing the output voltage with a first threshold voltage in the discontinuous mode and comparing the output voltage with the first and second threshold voltages in the continuous mode.

Accordingly, Appeltans does not teach or suggest turning off the switching transistors for pulses of a filter to regulate the output, but does teach varying the time they are on to regulate the output. Further, Appeltans does not teach maintaining an output voltage between upper and lower limit thresholds, but teaches switching states (i.e., changing the transistors on time) based on the result of the comparison of the output voltage with the first threshold and/or the second threshold.

The filter B101 of Poon is included in a variable induction control loop 115 and not in a PWM loop 105 that includes the feedback block 104. (column 4, lines 29-45) As such, the combined teachings of Appeltans and Poon do not teach or suggest an apparatus that includes a voltage converter and pulse frequency modulation unit as is presented claimed in claim 1. As claimed, the voltage converter converts a voltage of a first value to an output voltage of a second value. The pulse frequency modulation unit establishing an upper limit level and lower limit level for the output voltage by use of a

voltage mode control loop to maintain the output voltage from the converter near the second value determined by the upper and lower limit levels (i.e., the output voltage, not counting noise, stays between the upper and lower limits). The pulse frequency modulation unit further includes a filter that filters the feedback of the output voltage to detect sign changes at the filter when the upper and lower limit levels are detected and to skip a predetermined number of pulses from the filter after one of the sign changes to turn off the voltage converter. [emphasis added]

Based on the foregoing, the applicant believes that claim 1 overcomes the present rejection.

Claims 2-4 are dependent upon claim 1 and introduce additional patentable subject matter. The applicant believes that the reasons that distinguish claim 1 over the present rejection are applicable in distinguishing claims 2-4 and 7 over the same rejection.

4. Claims 5, 6, 17, and 18 have been rejected under 35 USC § 103 (a) as being unpatentable over Appeltans (U.S. Patent No. 5,552,694) in view of Bittner (U.S. Reissue Patent No. 37,609). The applicant respectfully disagrees with the Examiner's arguments supporting this rejection.

Claim 5 claims a direct current to direct current (DC-DC) converter that includes a converter circuit and a control circuit. The converter circuit converts a battery voltage to an output voltage, the converter circuit including a pair of switching transistors that, when enabled, switch alternately to have the battery voltage converted to produce the output voltage. The control circuit receives a feedback of the output voltage as part of a voltage mode control loop to maintain the output voltage within a specified value, the control circuit including an upper limit level detect circuit and a lower limit level detect circuit to detect upper and lower limit levels for the output voltage. The control circuit disables the converter circuit when the output voltage is at the upper limit level and enables the converter circuit when the output voltage is at the lower limit level to

maintain the output voltage between the upper and lower limit levels by use of the voltage mode control loop.

As stated above, Appeltans does not teach or suggest disabling the switching transistors as part of regulating the output voltage, but teaches change states (i.e., changing the on time of the switching transistors 2 and 11) based on how the output voltage compares with a first or a second threshold voltage.

Bittner teaches a current mode control loop that monitors the inductor current and the inductor voltage to determine when to turn on transistor 11 of Figure 1. Transistor 13 is not used in the PFM mode. In this mode, the PFM control circuit 7 regulates Vout by controlling the on and off states of switch 11 based on the inductor current and inductor voltage at node 12. The PFM control circuit 7 prevents switch 11 from turning on when Vout exceeds a predetermined nominal value. The PFM control circuit 7 compares a feedback voltage with a high voltage reference and a low voltage reference. When the feedback voltage exceeds the high voltage reference, the PFM control circuit 7 turns off switch 11 until the feedback voltage falls below the low voltage reference. When the feedback voltage is less than the high voltage reference, the on and off times of switch 11 are determined based on the inductor current and the inductor voltage. (column 4, lines 21 – 38)

Thus combining the current mode control loop of Bittner's PFM control circuit with the multiple state PFM of Appeltans fails to render the present invention of claim 5 obvious.

Claim 6 is dependent upon claim 5 and introduces additional patentable subject matter. The applicant believes that the reasons that distinguish claim 5 over the present rejection are applicable in distinguishing claim 6 over the same rejection.

Claim 17 includes similar limitations to claim 5 and, as such, the applicant believes that the reasons that distinguish claim 5 over the present rejection are applicable in distinguishing claim 17 over the same rejection.

Claim 18 is dependent upon claim 17 and introduces additional patentable subject matter. The applicant believes that the reasons that distinguish claim 17 over the present rejection are applicable in distinguishing claim 18 over the same rejection.

5. Claims 7 and 9 have been rejected under 35 USC § 103 (a) as being unpatentable over Appeltans (U.S. Patent No. 5,552,694) and Bittner (U.S. Reissue Patent No. 37,609) in view of Poon (U.S. Patent No. 6,188,209). The applicant respectfully disagrees with the Examiner's arguments supporting this rejection.

Based on the foregoing arguments, this combination of references does not teach or suggest the invention of claims 7 and 9. As such, the applicant believes that claims 7 and 9 overcome the present rejection.

6. Claims 11 and 12 have been rejected under 35 USC § 103 (a) as being unpatentable over Appeltans (U.S. Patent No. 5,552,694) in view of Malcolm (U.S. Patent No. 6,373,954) and Bittner (U.S. Reissue Patent No. 37,609). The applicant respectfully disagrees with the Examiner's arguments supporting this rejection.

Based on the foregoing arguments with respect to Appeltans and Bittner, combining the teaching of Malcolm still fails to teach or suggest the invention of claims 11 and 12. As such, the applicant believes that claims 11 and 12 overcome the present rejection.

7. Claims 19 and 20 have been rejected under 35 USC § 103 (a) as being unpatentable over Appeltans (U.S. Patent No. 5,552,694) and Bittner (U.S. Reissue

Patent No. 37,609) in view of Poon (U.S. Patent No. 6,188,209). The applicant respectfully disagrees with the Examiner's arguments supporting this rejection.

Based on the foregoing arguments, this combination of references does not teach or suggest the invention of claims 19 and 20. As such, the applicant believes that claims 19 and 20 overcome the present rejection.

For the foregoing reasons, the applicant believes that claims 1-20 are in condition for allowance and respectfully request that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present invention.

RESPECTFULLY SUBMITTED,

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